JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

KUKATPALLY - HYDERABAD – 500 085

EXAMINATION BRANCH

MOU-Foreign Collaborated Integrated Engineering Programme (USA)

SR INTERNATIONAL INSTITUTE OF TECHNOLOGY (VF) (MOU)

B.TECH II –I SEMESTER– R14- REGULAR AND SUPPLEMENTARY EXAMINATIONS, OCT/NOV- 2017

TIME TABLE

TIME: 10-00 AM TO 01-00 PM

BRANCH	DATE & DAY					
	20-10-2017 FRIDAY	23-10-2017 MONDAY	25-10-2017 WEDNESDAY	27-10-2017 FRIDAY	30-10-2017 MONDAY	01-11-2017 WEDNESDAY
ELECTRONICS AND COMMUNICATIONS ENGINEERING (32-E C E)	Mathematical Foundations of Computer Science	Pulse and Digital Circuits	Switching Theory and Logic Design	Signals and Systems	Electronic Devices & Circuits	-
COMPUTER SCIENCE AND ENGINEERING (33-C S E)	Mathematical Foundations of Computer Science – I	Probability & Statistics	Managerial Economics & Financial Accounts	Digital Logic Design	Electronic Devices & Circuits	Data structures through C++

NOTE:

i. ANY OMISSIONS OR CLASHES IN THIS TIME TABLE MAY PLEASE BE INFORMED TO THE CONTROLLER OF EXAMINATIONS, IMMEDIATELY.

ii. EVEN IF GOVERNMENT DECLARES HOLIDAY ON ANY OF THE ABOVE DATES, THE EXAMINATIONS SHALL BE CONDUCTED AS USUAL.

DATE: 23-09-2017

CONTROLLER OF EXAMINATIONS

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

KUKATPALLY - HYDERABAD – 500 085

EXAMINATION BRANCH

MOU-Foreign Collaborated Integrated Engineering Programme (USA)

SR INTERNATIONAL INSTITUTE OF TECHNOLOGY (VF) (MOU)

B.TECH II –I SEMESTER– R13- SUPPLEMENTARY EXAMINATIONS, OCT/NOV- 2017

TIME TABLE

TIME: 10-00 AM TO 01-00 PM

BRANCH	DATE & DAY					
	23-10-2017 MONDAY	27-10-2017 FRIDAY	30-10-2017 MONDAY	01-11-2017 WEDNESDAY	------	----------
COMPUTER SCIENCE AND ENGINEERING (33-C S E)	Probability & Statistics	Digital Logic Design	Electronic Devices & Circuits	Data structures through C++	----------	---------

NOTE:

i. ANY OMISSIONS OR CLASHES IN THIS TIME TABLE MAY PLEASE BE INFORMED TO THE CONTROLLER OF EXAMINATIONS, IMMEDIATELY.

ii. EVEN IF GOVERNMENT DECLARES HOLIDAY ON ANY OF THE ABOVE DATES, THE EXAMINATIONS SHALL BE CONDUCTED AS USUAL.

DATE: 23-09-2017

CONTROLLER OF EXAMINATIONS

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

KUKATPALLY - HYDERABAD – 500 085

EXAMINATION BRANCH

MOU-Foreign Collaborated Integrated Engineering Programme (USA)

SR INTERNATIONAL INSTITUTE OF TECHNOLOGY (VF) (MOU)

B.TECH II –I SEMESTER– R09- SUPPLEMENTARY EXAMINATIONS, OCT/NOV- 2017

TIME TABLE

TIME: 10-00 AM TO 01-00 PM

BRANCH	DATE & DAY					
	30-10-2017 MONDAY	----------	----------	----------	------	---------
ELECTRONICS AND COMMUNICATIONS ENGINEERING (32-E C E)	Electronic Devices & Circuits	--------	----------	----------	---------	--------

NOTE

i. ANY OMISSIONS OR CLASHES IN THIS TIME TABLE MAY PLEASE BE INFORMED TO THE CONTROLLER OF EXAMINATIONS, IMMEDIATELY.

ii. EVEN IF GOVERNMENT DECLARES HOLIDAY ON ANY OF THE ABOVE DATES, THE EXAMINATIONS SHALL BE CONDUCTED AS USUAL.

DATE: 23-09-2017

CONTROLLER OF EXAMINATIONS